Braille-line Flat 20

Principle

The Flat 20 is a compact block with 20 braille cells. It has an integrated drive electronic and an 200V power supply for the piezo actuators. It is stackable up to 4 blocks and up to 80 braille cells.

Communication

The communication is done by writing the output-shiftregister. Data are clocked in with the rising transition of the Clk signal.The content of this shiftregister is written to the output with the falling transition of the Strobe signal.
Due to the mechanical assembly the data bits are not ordered in braille modules and between the braille pins are empty bytes and the bits for the voltage setting. The ordering is shown in the attached list.
For the keys there is a separate input shift-register. The key inputs are transferred to the input-shiftregister while Strobe is high. With Strobe low they are clocked out at the rising transition of the Clk. There are 2 keys for every module, the even bit numbers are the keys in front.
The high voltage converter can be swiched off by applying a logic Low at the /shutdown pin to set the device in a low power condition. While shut-down and powered logic the keys can be read to end the shutdown.
When the shutdown mode is not used the shut-down pin can be left open because of a internal pullup resistor.

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sample program

CLK_L, CLK_H, STRB_H, STRB_L, DATA_H, DATA_L and DATA_IN are macros to set the appropriate Port Pin. wait() insert a little waittime to limit the speed of the communication

```
void ModulRdWr(unsigned char *data)
/*puts the pattern in the module and reads out the Cursor switchs*/
{
unsigned int i,j;
unsigned char outdat,indat;
unsigned char tmpCurPos=0xff;
/*send pattern to shift register*/
STROBE_H;

for (j=0;j<AnzBytes;j++)   //for all Outputbytes (incl. the voltagesetting)
 {
 outdat =*(data+AnzBytes-j-1);
 for (i=0;i<8;i++)
          {
          CLK_L;
          if (outdat & 1)    //Dataoutput
                    DATA_H;
          else
                    DATA_L;
          outdat>>=1;
          wait();              //short delay to limit speed
          CLK_H;
          wait();
          }
 }
STROBE_L;          //switch the content of outputshiftregister to the pins
                   //take the keypattern to the inputshiftregister
wait();
for (j=AnzModuls;j!=0;)     /*Cursor Routing einlesen*/
          {indat=0;
          for (i=0;i<2;i++)
                    {
                    wait();              //short wait to limit speed
                    CLK_L;
                    wait();
                    indat<<=1;
                    if (DATA_IN)      /*Data in*/
                              indat|=1;
                    else
                              indat&=~1;
                    CLK_H;
                    }
          j--;                 //next Mod
          CursorPattern[j]=indat;
          if (indat)           /*Cursor Key pressed*/
                    {if (indat &1)      /*Front Switch*/
                              tmpCurPos=j;
                    else
                              tmpCurPos=j+100;  /*Back = position +100*/
                    }
          CursorPos=tmpCurPos;
          }
   }
CLK_L;
STROBE_H;
}
```


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Datastring

Modul	Byte	Pin	Byte	Pin	Byte	Pin	Byte	Pin	Bit
	0	n.c.	**6**	n.c.	**12**	n.c.	**18**	Uout3	7
		n.c.		n.c.		n.c.		n.c.	6
		n.c.		n.c.		n.c.		Uout2	5
		n.c.		n.c.		n.c.		Uout1	4
		n.c.		n.c.		n.c.		n.c.	3
		n.c.		n.c.		n.c.		n.c.	2
		n.c.		n.c.		n.c.		n.c.	1
		n.c.		n.c.		n.c.		n.c.	0
20	**1**	7	**7**	3	**13**	2	**19**	1	7
		8		6		5		4	6
19		7		3		2		1	5
		8		6		5		4	4
18		7		3		2		1	3
		8		6		5		4	2
17		7		3		2		1	1
		8		6		5		4	0
16	**2**	7	**8**	3	**14**	2	**20**	1	7
		8		6		5		4	6
15		7		3		2		1	5
		8		6		5		4	4
14		7		3		2		1	3
		8		6		5		4	2
13		7		3		2		1	1
		8		6		5		4	0
12	**3**	7	**9**	3	**15**	2	**21**	1	7
		8		6		5		4	6
11		7		3		2		1	5
		8		6		5		4	4
10		7		3		2		1	3
		8		6		5		4	2
9		7		3		2		1	1
		8		6		5		4	0
8	**4**	7	**10**	3	**16**	2	**22**	1	7
		8		6		5		4	6
7		7		3		2		1	5
		8		6		5		4	4
6		7		3		2		1	3
		8		6		5		4	2
5		7		3		2		1	1
		8		6		5		4	0
4	**5**	7	**11**	3	**17**	2	**23**	1	7
		8		6		5		4	6
3		7		3		2		1	5
		8		6		5		4	4
2		7		3		2		1	3
		8		6		5		4	2
1		7		3		2		1	1
		8		6		5		4	0

serial output byte 0 bit 7 first

Power-relation

Uout3	Uout2	Uout1	Uout [V]
0	0	0	155
0	0	1	162
0	1	0	168
0	1	1	174
1	0	0	177
1	0	1	184
1	1	0	191
1	1	1	199

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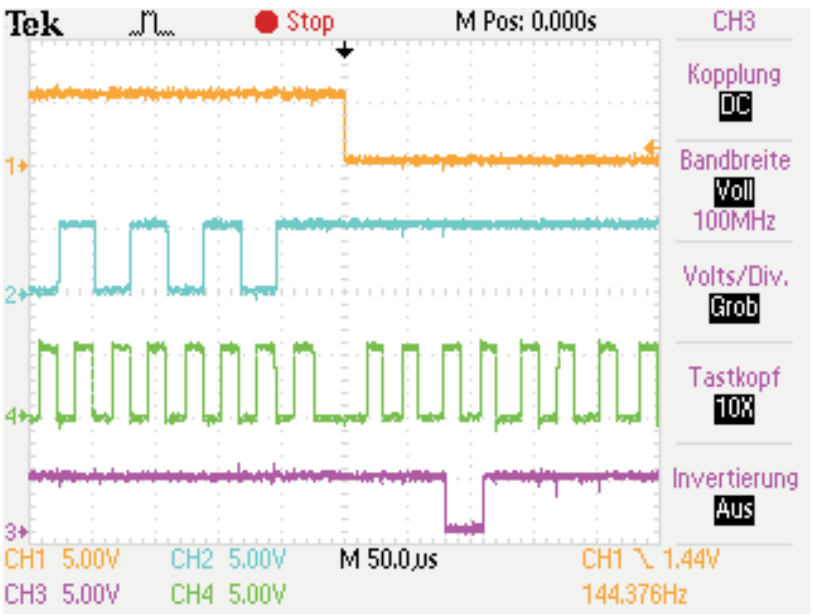
Signal Diagram



This are the signals around the Strobe H transisiton

channel 1	yellow	Strobe
channel 2	blue	data to module (piezo output)
channel 3	purple	data frome module (key read)
channel 4	green	Clk

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